REMARKS

Claims 1 through 7 remain pending. In response to the Office Action dated June 14, 2005, claim 1 has been amended. Care has been taken to avoid adding new matter. Favorable reconsideration and allowance of the application are respectfully solicited.

Objection has been made to claim 1 for the reason that the definition of variables N and M are recited at improper locations. In response, claim 1 has been amended to recite the definitions of "N" and "M" after their respective occurrences. In addition, "N" has been defined to be a natural number greater than two. It is submitted that claim 1 as amended causes no confusion. Withdrawal of the objection is respectfully solicited.

Claims 1 through 7 have been rejected under 35 U. S. C. § 102(e) as being unpatentable over U.S. patent 6,888,776 (Watanabe). The rejection is respectfully traversed.

Independent claim 1 recites, *inter alia*, the following:

> a first local control circuit, in a refresh mode, starting an operation of successively selecting rows of said first memory cell array in response to a first refresh end signal received from an (M−1)th sub-memory block and instructing a refresh start to an (M+1)th sub-memory block when said operation of successively selecting rows ends . . . .

Independent claim 6 recites, *inter alia*, the following:

> a local control circuit performing an operation of successively selecting rows of said memory cell array in response to an end of a refresh operation in a sub-memory block at a previous stage which precedes by one in refresh-circulating order of said plurality of sub-memory blocks, and
>
> a refresh cycle period in each of said plurality of memory blocks is determined depending on a number of said sub-memory blocks included in said first memory block.

Watanabe does not disclose or suggest a first local control circuit, in a refresh mode, starting an operation of successively selecting rows of the first memory cell array in response to

a first refresh end signal received from an (M-1)th sub-memory block and instructing a refresh start to an (M+1)th sub-memory block when said operation of successively selecting rows ends as recited claim 1 or similar requirements of claim 6.

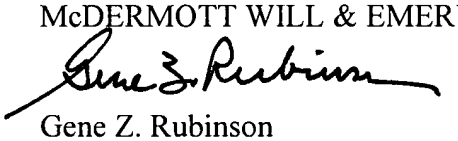
Watanabe only discloses that the refresh counter 204 is reset by the final refresh detection signal SMXRF corresponding to the last sub-memory block MB11 in Fig. 35 (see column 50, lines 25-29). Although it is unnecessary to change the configuration of the refresh counter 204, the refresh counter 204 must deal with the redundant bits that are expected to be extended. The local control circuit recited in claim 1 is not included in each of memory blocks MB1-MB10 placed between memory block MB0 and memory block MB11 in Fig. 34 of Watanabe. Watanabe and the subject application both relate to technology for generating various refresh cycle times. The claimed semiconductor memory device, however, has a smaller refresh counter than Watanabe's refresh counter with redundant bits.

Watanabe does not disclose nor suggest a local control circuit performing an operation of successively selecting rows of said memory cell array in response to an end of a refresh operation in a sub-memory block at a previous stage which precedes by one in refresh-circulating order of said plurality of sub-memory blocks in claim 6. Watanabe only discloses that the refresh counter 204 is reset by the final refresh detection signal SMXRF corresponding to the last sub-memory block MB11 in Fig. 35 (see column 50, lines 25-29). Although it is unnecessary to change the configuration of the refresh counter 204, the refresh counter 204 must deal with the redundant bits that are expected to be extended. The local control circuit in claim 6 is not included in each of memory blocks MB1-MB10 placed between memory block MB0 and MB11 in Fig. 34 of Watanabe.

Accordingly, it is submitted that independent claims 1 and 6, and their dependent claims 2 through 5 and 7, are not met by the Watanabe disclosure pursuant 35 U. S. C. § 102, nor rendered obvious therefrom pursuant 35 U. S. C. § 103. Withdrawal of the rejection and allowance of the application are respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP



Gene Z. Rubinson
Registration No. 33,351

Please recognize our Customer No. 20277 as our correspondence address.

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 GZR:lnm
Facsimile: 202.756.8087
Date: August 29, 2005

WDC99 1125883-1.067161.0111